REMARKS

The Office Action of December 15, 2005 has been received and its contents carefully considered.

The present Amendment revises all of the claims except dependent claims 3 and 9, which are being cancelled as redundant in view of the changes to the independent claims.

Turning now to section 2 of the Office Action, the drawing objection is respectfully traversed. Element 9 in Figure 1, element 33 in Figure 3, and element 35 in Figure 4 have similar functions, so it is appropriate for the application to refer to them using the same name ("clock dividing ratio changing circuit"). However, they are not exactly the same, so it is also appropriate for them to bear different reference numbers. As will be seen from Figure 1, the circuit 9 receives four "clock dividing ratio change request signals," while the circuit 33 in Figure 3 receives only two. The internal construction of circuits 9 and 33 must therefore differ, so these elements should not bear the same reference number. The circuit 35 in Figure 4 receives four "clock dividing ratio change request signals," but it would nevertheless be inappropriate for it to have the same reference number as the corresponding circuit in Figure 1. The reason is that circuit 35 in Figure 4 also receives a memory access signal 32, and hence the internal construction of circuit 35 is not exactly the same as that of circuit 9 in Figure 1.

Similarly, the "access wait changing circuit" 29 in Figure 3 receives only one input signal but the "access wait changing circuit" 34 in Figure 4 receives four input signals. It therefore properly carriers a different reference number.

The Office Action rejects all of the claims for obviousness based on a published application by Lee et al (hereafter simply "Lee") in view of a patent to Flannery. For the

reasons discussed below, however, it is respectfully submitted that the inventions defined by independent claims 1 and 7 are patentable over these references.

The Lee reference discloses an arrangement for varying the frequency of a clock signal supplied to a memory in accordance with the priorities assigned to devices that access the memory. The Flannery reference discloses an arrangement for adjusting the minimum number of clock cycles required for a memory access when the clock speed of a computer system is changed.

Furthermore, claim 1 recites a CPU that is configured to operate with one of a plurality of clock frequencies that are determined in accordance with clock change signals derived from interrupt signals, and "a clock frequency changer for conveying a clock signal having said one of the plurality of clock frequencies to the CPU based on" a selected one of the clock change signals." The Lee reference does not convey a clock signal having the desired frequency to Lee's memory. Instead, Lee uses a phase locked loop to generate the desired frequency. An ordinarily skilled person who wanted to improve Lee's arrangement in some way would not have had an incentive to supply Lee's clock signal to a CPU rather than a memory, and also would not have had an incentive to convey a clock signal having the desired frequency to a CPU instead of generating the desired frequency with a phase locked loop.

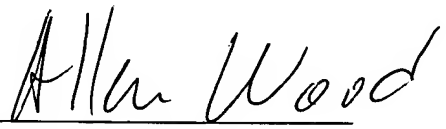
The disclosure of the Flannery reference does not fill in what is missing from Lee. Accordingly, it is respectfully submitted that both references together would not have led an ordinarily skilled person to the invention now defined by claim 1.

Independent claim 7 is similar to claim 1 but includes recitations in "means-plus-function" form. For the same reasons discussed above with respect to claim 1, though, it is respectfully submitted that claim 7 is patentable over Lee and Flannery.

The remaining claims depend from the independent claims discussed above and recite additional limitations to further define the invention, so they are patentable along with their independent claims. It is nevertheless noted that claim 2 (depending from claim 1) provides generally that the "clock frequency changer" of claim 1 is inoperative when a detector determines that a memory access is currently being performed, and conveys the cock signal having said one of the plurality of clock frequencies to the CPU together with information that includes information about memory access timing "when the detector determines that a memory access is not currently being performed." Dependent claim 8 is similar, but depends from independent claim 7. The inventions defined by dependent claims 2 and 8 are not suggested by Lee and Flannery. The timing of a memory access is adjusted in the Flannery reference, but nothing in the reference would have taught an ordinarily skilled person that a change in the clock speed of a CPU and the access timing for a memory should be held in abeyance while a memory access is taking place.

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



Allen Wood
Registration No. 28,134
Customer number 23995
Rabin& Berdo, P.C.
Suite 500
1101 14th Street, N.W.
Washington, DC 20005
(202) 326-0222 (telephone)
(202) 408-0924 (facsimile)
(202) 408-5297 (facsimile)

AW:rw